41

2675

Attorney's Docket No.: 07977-211003 / US3517D1D1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Yamazaki, et al.
Serial No. : 09/924,337
Filed : August 6, 2001
Title : SEMICONDUCTOR DEVICE

Art Unit : 2675
Examiner : Alecia Diane Nelson

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO ACTION OF JUNE 4, 2004

In response to the Office Action of June 4, 2004, please consider the following remarks.

Claims 1-14 and 16-34 are pending, with claims 1, 16, 18, 20, 21, 27, 30 and 33 being independent. Claim 15 was previously cancelled.

Claims 1-14 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,818,068 to Sasaki et al. (Sasaki) in view of U.S. Patent No. 5,550,070 to Funai et al. (Funai). Claims 16-19, 21, 23, 24, and 26-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of U.S. Patent No. 5,888,857 to Zhang et al.(Zhang). Claims 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of U.S. Patent No. 5,959,599 to Hirakata (Hirakata).

Regarding the rejection of independent claim 1 under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Funai, Applicant respectfully submits that neither Sasaki nor Funai, nor any proper combination of the two, discloses or properly suggests all of the limitations of independent claim 1. Further, Applicant submits that the rejection of at least claim 1 fails to provide proper motivation to combine Sasaki and Funai in the proposed manner.

For example, claim 1 recites (with emphasis added):

> A semiconductor device comprising:
> a pixel matrix circuit including at least source lines and gate lines;
> a driver circuit including at least a source line driver circuit for driving the source lines and a gate line driver circuit for driving the gate lines; and
> a logic circuit for processing a signal required for driving the driver circuit and a signal including image information transmitted to the pixel matrix circuit,
> wherein the pixel matrix circuit, the driver circuit and the logic circuit are disposed over the same substrate,
> wherein the pixel matrix circuit, the driver circuit, and the logic circuit are constituted by a plurality of thin film transistors, each having an active layer comprising crystalline silicon,
> wherein the active layer of each of the plurality of thin film transistors comprises a plurality of rod-shaped crystals extending in one direction, and
> wherein the logic circuit includes at least one selected from the group consisting of a phase comparator, a low pass filter, a voltage controlled oscillator, a frequency divider, a horizontal scanning oscillator, a vertical scanning oscillator, a D/A converter, an I/O port, a differential amplifier, an operational amplifier, a comparator and a memory.

Paragraph 3 of the Office Action asserts that Sasaki discloses a "driver circuitry (84, 85) for driving the source lines and gate lines (66, 67), and a logic circuit for processing a signal required for driving the driver circuits...", and appears to refer to the "buffer circuit" and/or "sample/hold circuit" of column 12, lines 27-50 of Sasaki for this disclosure. Applicant respectfully submits, however, that paragraph 3 of the Office Action is unclear as to exactly what elements of Sasaki are asserted to correspond to Applicant's claimed "logic circuit," as claimed, particularly since Sasaki does not appear to teach a logic circuit separately from the driver circuit(s) of that reference. Therefore, and since Funai does not disclose or suggest such a logic circuit, Applicant requests that the Examiner specifically identify the elements of Sasaki that are thought to correspond to Applicant's claimed logic circuit.

In particular, claim 1 specifies, as highlighted above, that the claimed logic circuit includes at least one selected from the recited group "...consisting of a phase comparator, a low

pass filter, a voltage controlled oscillator, a frequency divider, a horizontal scanning oscillator, a vertical scanning oscillator, a D/A converter, an I/O port, a differential amplifier, an operational amplifier, a comparator and a memory." Applicant submits that Sasaki does not disclose or suggest such a logic circuit selected from the recited group, nor does the Office Action even allege that Sasaki discloses or properly suggests this feature of claim 1. Further, as discussed in more detail below, Funai does not cure this defect of Sasaki, and is not alleged to cure this defect of Sasaki.

Further, claim 1 recites that "the active layer of each of the plurality of thin film transistors comprises a plurality of rod-shaped crystals extending in one direction." Regarding this claim feature, paragraph 3 of the Office Action asserts that Sasaki "...teaches that the crystals grow in a substantially parallel direction." Applicant respectfully disagrees, since, in fact, Sasaki does not appear to provide such a teaching. For example, Sasaki discloses that an active layer in a pixel matrix circuit is not the same as an active layer in the driver circuit, so there is no rationale to think or assume that such different active layers include parallel crystal growth (nor does Sasaki appear to assert such parallel crystal growth).

Additionally, paragraph 3 of the Office Action admits that Sasaki does not disclose or suggest "rod-shaped crystals," and relies on Funai for this teaching by asserting that, "a leak current flowing between the shaped crystals becomes less and thereby further increasing the display characteristics and performance of the display device." In response, Applicant submits that motivation to combine must come from the cited references, or from knowledge generally available in the art. Here, neither Sasaki nor Funai provides support for this reason to combine (i.e., neither reference discloses or suggests that a leak current flowing between the shaped crystals is reduced by way of using rod-shaped crystals), and the Office Action does not assert that the stated rationale stems from generally-available knowledge (although stating that rod-shaped crystals are generally known). Therefore, Applicant submits that no proper motivation to combine Sasaki and Funai in the proposed manner has been provided.

In summary regarding claim 1, then, Applicant submits that (1) the Office Action fails to establish that either Sasaki or Funai, or any proper combination of the two, discloses or suggests

a logic circuit formed on the same substrate as a driver circuit, as claimed, where the logic circuit includes one selected from the recited group; (2) Sasaki does not disclose or properly suggest "crystals grow(ing) in a substantially parallel direction" within the active layers of the thin film transistors of that reference; and (3) neither Sasaki nor Funai (nor any proper combination thereof) provides the stated motivation to modify Sasaki to use rod-shaped crystals, as claimed.

Regarding the rejection of independent claims 16, 18, 21, 27, 30, and 33 under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Zhang, Applicant respectfully submits that each of these claims recite the limitation that a logic circuit is formed on the same substrate as a driver circuit, and that the logic circuit is selected from a defined group. Neither Sasaki nor Zhang, nor any proper combination of the two, discloses or suggests a logic circuit from the recited group being formed on the same substrate as a driver circuit, so that claims 16, 18, 21, 27, 30, and 33 are allowable for at least this reason.

Further, claims 16 and 27 specify subthreshold coefficients of the plurality of N-channel thin film transistors and the plurality of P-channel thin film transistors as being within a range of 60 to 100 mV/decade. Neither Sasaki nor Zhang, nor any proper combination of the two, discloses or suggests this feature, nor does the Office Action assert that Sasaki and/or Zhang discloses or suggests this feature. The Office Action does discuss alleged teachings of Zhang regarding ranges of the field effect mobility of the TFT(s) of that reference, but does not discuss how the recited ranges are thought to correspond to the recited subthreshold coefficient ranges of claims 16 and 27.

Also, claims 18 and 30 recite that wherein "...dimensions of the plurality of thin film transistors are made different depending upon required electrical characteristics." Neither of Sasaki nor Zhang, alone or in combination, discloses or properly suggests this feature. In fact, although claims 18 and 30 are included in the listing of rejected claims in paragraph 4, neither of these claims is actually discussed in the Office Action.

Also, claim 21 recites, "wherein a plurality of circuits constituting the pixel matrix circuit, the driver circuit and the logic circuit include at least two kinds of circuits which are different from each other in at least one of a driving frequency and an operating voltage."

Neither of Sasaki nor Zhang, alone or in combination, discloses or properly suggests this feature. In fact, although claim 21 is included in the listing of rejected claims in paragraph 4, it is not actually discussed in the Office Action.

Further, claim 33 recites, "wherein a thickness of a first gate insulating film of one of the plurality of thin film transistors which is required to drive a circuit of 0.1 GHz or higher is 500 Å or thinner, and a thickness of a second gate insulating film of one of the plurality of thin film transistors which is driven by an operation voltage of 10V or greater is 1000 Å or thicker." As above, neither of Sasaki nor Zhang, alone or in combination, discloses or properly suggests this feature. Also as above, although claim 33 is included in the listing of rejected claims in paragraph 4, it is not actually discussed in the Office Action.

Regarding the rejection of independent claim 20 under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Hirakata, Applicant respectfully submits that, as above, claim 20 recites the limitation that a logic circuit is formed on the same substrate as a driver circuit, and that the logic circuit is selected from a defined group. Neither Sasaki nor Hirakata, nor any proper combination of the two, discloses or suggests a logic circuit from the recited group being formed on the same substrate as a driver circuit, so that claim 20 is allowable for at least this reason.

Further, claim 20 recites, similarly to claim 33, that "a thickness of a first gate insulating film of one of the plurality of thin film transistors which is required to drive a circuit of 0.1 GHz or higher is 500 Å or thinner, and a thickness of a second gate insulating film of one of the plurality of thin film transistors which is driven by an operation voltage of 10V or greater is 1000 Å or thicker." As above, neither of Sasaki nor Hirakata, alone or in combination, discloses or properly suggests this feature.

In paragraph 5, the Office Action states that, "Sasaki fails to teach the amount of voltage needed to drive the gate insulating film of the TFT when it is at a certain thickness," and that, "it would be obvious ... to apply a higher operating voltage to the gate insulating film when the film is thicker as opposed to the amount applied when the film is thinner." However, without necessarily agreeing with these statements, Applicant submits that claim 20 recites the use of

TFTs having gate insulating films with different thicknesses, and that neither Sasaki nor Hirakata, nor any combination of the two, discloses or properly suggests this feature. Similar comments apply to claim 33, as that claim is discussed above.

Accordingly, independent claims 1, 16, 18, 20, 21, 27, 30, and 33 are thought to be allowable for at least the above reasons, so that their dependent claims 2-14, 17, 19, 22-26, 28, 29, 31, 32, and 34 are thought to be allowable for at least the same reasons.

Based on the above, all claims are believed to be in condition for allowance, and such action is hereby requested in the Examiner's next official communication.

Enclosed is a $110.00 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: October 4, 2004

William G. Hughes, Jr.
Reg. No. 46,112

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331